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UNITED STATES PATENT APPLICATION
FOR

METHODS OF SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT PACKAGE

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CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit and is a divisional of Application No. 09/665,034, filed September 9, 2000, now pending which is a continuation of Application No. 09/153,630, filed September 15, 1998, now issued as U.S. Patent No. 6,153,829.

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an integrated circuit package.

2. DESCRIPTION OF RELATED ART

Integrated circuits are typically housed within a package which has a plurality of external contacts that are soldered to a printed circuit board. The package may also have a number of internal bond pads that are connected to corresponding pads of the integrated circuit by bond wires or a tape automated bonding (TAB) tape. The internal bond pads may be connected to the external contacts by routing layers and busses within the package. The busses and routing layers have conductive planes and traces that are dedicated to the power/ground busses and digital signal lines of the integrated circuit, respectively. By way of

example, a conventional package may have a first bus layer dedicated to power, one or more routing layers dedicated to digital signals and a second bus layer dedicated to ground.

The various conductive layers are spatially located within different planes in the package. The layers are typically interconnected by conductive vias formed within the package. The bond pads may also be connected to the internal conductive layers by vias. Vias are typically formed by creating a hole in the dielectric package material and then plating the hole with a conductive material such as copper. The plating process is a relatively time consuming and expensive step. For this reason it is desirable to create an integrated circuit package with a minimal number of vias.

Some integrated circuits require power at different voltage levels. For example, an integrated circuit may require both 3.3 V and 2.0 V power. The additional voltage level requires an additional conductive power plane within the package. The second power plane can be created by forming an additional conductive layer within the package. The additional conductive layer requires more vias to connect the second power plane to the bond pads. It would be desirable to provide a dual voltage integrated circuit package which minimized the number of vias required to interconnect the pads and conductive layers of the package.

U.S. Patent No. 5,557,502, issued to Banerjee et al., discloses an integrated circuit package which has a

conductive strip that wraps around an edge of a bond shelf to interconnect a power bus to one or more bond pads on the shelf. The conductive strip is typically formed by initially masking all surfaces of the integrated circuit package except for the edge, and then dipping the package into a plating bath of copper. The plating bath plates copper onto the edge on the bond shelf.

The conductive copper strip extends continuously along the entire edge of the bond shelf. Because of this only one voltage level can be supplied to the contact pads located on the bond shelf with the plated edge. To provide more design flexibility it would be desirable to connect multiple power/ground planes to the bond pads on the bond shelf with the conductive strip.

SUMMARY OF THE INVENTION

The present invention is an electronic package that may include a first bond pad and a second bond pad located on a bond shelf. The bond shelf may have an edge. The package may have a first conductive bus that may be connected to the first bond pad by a first conductive strip that extends along the edge of the bond shelf. The package may also have a second conductive bus that may be connected to the second bond pad by a second conductive strip that extends along the edge of the bond shelf.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an integrated circuit package of the present invention;

Figure 2 is a top sectional view of the package;

Figure 3 is a top cross-sectional view of the integrated circuit package showing a pair of power busses within the same plane of the package;

Figure 4 is an enlarged perspective view of a bond shelf of the package showing a pair of conductive strips that wrap around the edge of a bond shelf to connect a pair of conductive busses to bond pads located on the shelf;

Figure 5 is a perspective view showing the package masked by a plating resist material;

Figure 6 is a side view showing the package within a plating bath;

Figure 7 is an enlarged view of a conductive strip that extends along an edge of a bond shelf.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 1-3 show an integrated circuit package 10 of the present invention. Mounted to the package 10 is an integrated circuit 12. Although an integrated circuit 12 is shown and described, it is to be understood that the package 10 may house any passive or active electrical device. The integrated circuit 12 has a plurality of bond pads 14 that are connected to corresponding bond pads 16 of a package housing 11. The bond pads 14 and 16 may be connected by bond wires 17 or a tape automated bonding (TAB) tape (not shown). The bond pads 16 may be located on a first bond shelf 18, a second bond shelf 20 and a third bond shelf 22. Although three bond shelves are shown and described, it is to be understood that the package 10 may have any number of bond shelves.

The bond pads 16 of the first bond shelf 18 are connected to a pair of power busses 24 and 26 within the package. The busses 24 and 26 are separated and located within the same horizontal plane of the package. By locating both power busses 24 and 26 within the same plane the present invention provides a package that may require less layers than a package that has two power busses located within different layers of the package.

The package 10 may also have one or more layers of routing traces 28 and a ground bus 30 dedicated to the digital signal lines and ground of the integrated circuit 12, respectively. The busses 24, 26 and 30, and traces 28 are connected to a plurality of contacts 32 that are attached to surface pads 33 located on a bottom surface of the package 10. The contacts 32 may be solder balls that are reflowed onto a printed circuit board 34. By way of example, the printed circuit board 34 may be a motherboard of a computer that contains a power supply(ies) 36 that provides two different voltage levels of power.

In one embodiment, the power bus 24 is connected to one voltage level, such as 3.3 V, and the other power bus 26 can be connected to a second voltage level, such as 2.0 V. In this manner the package provides two different voltage levels to the integrated circuit 12. Although the busses 24 and 26 are described as being both dedicated to power, it is to be understood that one bus may be connected to power and the other bus may be connected to ground. Such a configuration may reduce the capacitance of the package 10. Additionally, although solder balls 32 are shown and described, it is to be understood that the package 10 may have other types of contacts such as pins (not shown) that are soldered to the printed circuit board 34.

The bond pads 16 and layers of busses 24 and 26, routing traces 28, bus 30, and contacts 32 may all be

interconnected by vias 38. The busses 24 and 26 may include clearance spaces 42 that electrically isolate the busses 24 and 26 from the vias 38. Additionally, the busses 24 and 26 are also separated by spaces 43.

Figure 4 shows a first conductive strip 44 and a second conductive strip 46 that wrap around an edge of the first bond shelf 18 to connect the bond pads 16 to the power busses 24 and 26. The conductive strips 44 and 46 can be separated by a pair of notches 48 formed in the first bond shelf 18. Some of the bond pads 16 are connected to bus 24 by conductive strip 44 while other bond pads 16 are connected to bus 26 by strip 46. The separate strips allow the bond pads 16 on the first bond shelf 18 to be connected to two different voltage levels. The other bond pads 16 on the first bond shelf 18 may be interconnected to other layers and/or contacts 32 by vias 38.

In the preferred embodiment, the package 10 is constructed with a laminated printed circuit board process. The ground layer 30 can be formed on a dielectric substrate with conventional photolithographic techniques. A second substrate may be placed on the ground layer 30. The layer may have a plurality of holes used for the formation of the vias 38. The second substrate may contain copper layers that are etched to form the routing traces 28 and bond pads 16. Additional substrates may be added to create the busses 24 and 26, and bond pads 16. The vias 38 can then

be formed with a plating process. The substrates are then "auto-claved" to form the package housing 11.

The conductive strips 44 and 46 can be formed by initially masking off all surfaces of the package housing, except the edge 49 of the first bond shelf 18 with a plating resist maskant 50, as shown in Figure 5. The masked housing can then be dipped into a plating bath 52 as shown in Figure 6. The plating bath 52 plates a conductive material such as copper onto the edge 49 of the first bond shelf 18. The maskant 50 is then removed and the notches 48 can be drilled into the edges of the first bond shelf 18 to separate the plated material into the first and second conductive strips 44 and 46. All exposed copper surfaces may then be plated with gold.

As shown in Figure 7, portions 54 of the conductive strips 44 and 46 may extend onto the first bond shelf 18 to connect to a bonding pad 16. The extra portions 54 may further anchor the conductive strips 44 and 46 to the housing and reduce the likelihood of delamination during the drilling process. The additional portions 54 can be formed by not masking the end of the first bond shelf 18 so that conductive material plates onto the shelf.

Referring to Figs. 1 and 2, after the strips 44 and 46 are formed, the integrated circuit 12 may be mounted onto the package and connected to the bond pads 16. The integrated circuit 12 may then be enclosed with an

encapsulant 56. The contacts 32 are attached to the surface pads 33 to complete the package 10.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.